

## Introduction

The cis the subject of this data sheet. However, other members of this device family are discussed in this paragraph for reference. Data sheets are available for the NGCL3590, NGCL3571, and NGCP3580. NGC3571/3580/3590 series is a family of radiation hardened 16:1 Analog Multiplexers designed by the Northrop Grumman Advanced Technology Center, Baltimore, MD, using $5 \mathrm{~V}, 10 \mathrm{~V}$ and 30 V CMOS technologies on Silicon On Insulator (SOI) starting material. The NGCL3571 and NGCL3590 use a low voltage ( $10 \mathrm{~V} / 5 \mathrm{~V}$ ) process and feature CMOS analog switches. The NGCP3580 uses a high voltage (30V) process and features PMOS analog switches. CMOS analog switches result in rail to rail operation with minimal variation in switch impedance. CMOS switches offer the advantage of Iow switch impedance (<500 Ohms) and fast access time (<500 ns) over temperature, voltage and radiation level. All switches maintain high OFF state impedance even under power down conditions for redundant applications. SOI technology coupled with special design techniques makes this part immune to latch-up. Part has no latched data and is not subject to Single Event Upset (SEU) failures.

## Features

- 10 V CMOS using SOl starting material
- Recommended Operating Voltages $-\mathrm{V}+-\mathrm{V}-=10 \mathrm{~V}$, Vdig $=+5 \mathrm{~V}(+/-10 \%)$ [ $\mathrm{V}-=0 \mathrm{~V}, \mathrm{~V}+=+10 \mathrm{~V}$ or $\mathrm{V}-=-5 \mathrm{~V}, \mathrm{~V}+=+5 \mathrm{~V}$ ]
- Total Dose up to 300 krad (Si)
- No Single Event Upset (SEU) effects (no latched data)
- CMOS analog switching allows rail to rail operation and low switch impedance
- < 500 Ohm nominal CMOS switch impedance
- < 1000 Ohm worst case CMOS switch impedance
- Break before make switching
- < 500 ns access time over temperature and post rad
- > 100 MOhm OFF switch impedance
- High OFF state impedance maintained under powered down conditions - ideal for redundant applications
- Low power dissipation: <100 $\mu \mathrm{A}$ standby current
- > 1 kV electrostatic discharge protection (Human Body Model)
- Available in 28 pin flatpacks or bare die
- Full military operating temperature range, screened to specific test methods for commercial, Class B, or modified Hi Rel.


## Absolute Maximum Ratings

|  | NGCL3571 | UNITS |
| :--- | :---: | :---: |
| Supply Voltage, V+ to V- | 15 | volts |
| Supply Voltage, V+ to GND | 7.5 | volts |
| Supply Voltage, VDIG to GND | 7.5 | volts |
| Digital input overvoltage range min | -0.5 |  |
| Digital input overvoltage range max | $\mathrm{V}_{\text {DIG }}+0.5$ | volts |
| Analog input overvoltage range min | V- minus 10 | volts |
| Analog input overvoltage range max | V+ plus 10 | volts |
| Storage Temperature |  |  |
| Min | -65 | deg C |
| Max | 150 | deg C |


|  | 1 |  | 28 | Out |
| :---: | :---: | :---: | :---: | :---: |
| nc | 2 |  | 27 | v. |
| nc | 3 |  | 26 | IN8 |
| W16 | 4 |  | 25 | IN7 |
| \|N15 | 5 |  | 24 | IN6 |
| \|N14 | 6 |  | 23 | IN5 |
| N13 | 7 | Flatpack | 22 | IN4 |
| \|N12 | 8 |  | 21 | IN3 |
| 11 | 9 |  | 20 | IN2 |
| IN10 | 10 |  | 19 | IN1 |
| 1 N 9 | 11 |  | 18 | ENABIE |
| GND | 12 |  | 17 | AdDr AO |
| volg | 13 |  | 16 | AdDr Al |
| DDR A3 | 14 |  | 15 | adr A2 |
| Pinout |  |  |  |  |
| (Top View) |  |  |  |  |

## Functional Diagram



## DC Operating Characteristics: NGCL3571

Recommended Operating Conditions: $\mathrm{V}+-\mathrm{V}-=10 \mathrm{~V}(+/-10 \%)[\mathrm{V}-=\mathrm{OV}, \mathrm{V}+=+10 \mathrm{~V}$ or $\mathrm{V}-=-5 \mathrm{~V}, \mathrm{~V}+=+5 \mathrm{~V}](\mathrm{Vdig}=+5 \mathrm{~V}, \mathrm{~V}+/-=-10 \%)$

| Symbol | Description | 25C Max | $\begin{aligned} & -55 \text { to }+125 \text { C Max } \\ & \text { (Note 2) } \end{aligned}$ | Units |
| :---: | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\text {SUPPIY }+}$ | V+ supply current | 500 | 500 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {SUPPIY }}$ | V-supply current | 500 | 500 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {STBY }+}$ | V+ standby current | 500 | 500 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {STBY- }}$ | V-standby current | 500 | 500 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {AH }}$ | input leakage | 1 | 1 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {AL }}$ | input leakage | 1 | 1 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {S(IFf)- }}$ | leakage into source of off switch $-v_{\text {in }}$ | 50 | 500 | nA |
| $\mathrm{I}_{\text {S(Off) }+}$ | leakage into source of off switch $+\mathrm{v}_{\text {in }}$ | 50 | 500 | nA |
| $\mathrm{I}_{\text {SIOFF, Poweroff }}$ | leakage into source of off switch, $\mathrm{V}+=\mathrm{V}-=0$ | 50 | 500 | nA |
| $\mathrm{I}_{\text {SIOFF }} \mathrm{OV}+$ | Isoff with overvoltage | 1000 | 1000 | nA |
| $\mathrm{I}_{\text {SIOFF }} \mathrm{OV}-$ | Isoff with overvoltage | N/A (Note 1) | N/A (Note 1) | nA |
| $\mathrm{I}_{\text {D(OFF) }} \mathrm{OV}+$ | leakage into drain of off switch with overvoltage | 1 | 10 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {D(OFF) }} \mathrm{OV}-$ | leakage into drain of off switch with overvoltage | N/A (Note 1) | N/A (Note 1) | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {D(OFF) }}+$ | leakage into drain of off switch | 50 | 5000 | nA |
| $\mathrm{I}_{\text {D(OFF) }}$ - | leakage into drain of off switch | 50 | 5000 | nA |
| $\mathrm{I}_{\text {D(ON) }}+$ | leakage from on driver into switch $+\mathrm{V}_{\text {in }}$ | 50 | 5000 | nA |
| $\mathrm{IDION)}^{\text {- }}$ | leakage from on driver into switch $-v_{\text {in }}$ | 50 | 5000 | nA |
| $\mathrm{R}_{\text {DSION }} 5$ | switch on resistance $+\mathrm{V}_{\text {in }}$ | 1000 | 1000 | ohms |
| $\mathrm{R}_{\text {DS (IN) }} 0$ | switch on resistance $-\mathrm{V}_{\text {in }}$ | 1000 | 1000 | ohms |
| $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}-5$ | switch on resistance $\mathrm{v}_{\text {in }}=0$ | 1000 | 1000 | ohms |

Note 1: The NGCL3571 does not allow undervoltage operation and maximum recommended undervoltage condition is 0.5 V below V -.

Note 2: $\quad$ Deliverable die are not tested cold and hot. Performance over temperature is guaranteed by design. Die from each wafer are sampled and tested over temperature in packages during the Class K screening.

## AC Operating Characteristics: NGCL3571

Guaranteed but not tested
Recommended Operating Conditions: $\mathrm{V}+-\mathrm{V}-=10+/-10 \%[\mathrm{~V}-=\mathrm{OV}, \mathrm{V}+=+10 \mathrm{~V}$ or $\mathrm{V}-=-5 \mathrm{~V}, \mathrm{~V}+=+5 \mathrm{~V}](\mathrm{Vdig}=+5 \mathrm{~V}+-10 \%)$

| Symbol | Description | Conditions | -55 to +125C Limits |  | Type | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Max |  |  |
| $\mathrm{C}_{\text {A }}$ | capacitance, digital Input | $\begin{aligned} & V+=V-=O V \\ & f=1 M H z, T A=25 C \end{aligned}$ |  | 7 | 1 | pF |
| $\mathrm{C}_{\text {Sloff }}$ | capacitance, channel Input | $\begin{aligned} & V+=V-=O V \\ & f=1 M H z, T A=25 C \end{aligned}$ |  | 5 | 3 | pF |
| $\mathrm{C}_{\text {D(OFF) }}$ | capacitance, channel output | $\begin{aligned} & V+=V-=O \\ & f=1 \mathrm{MHz}, \mathrm{TA}=25 \mathrm{C} \end{aligned}$ |  | 50 | 30 | pF |
| $V_{\text {ISO }}$ | off isolation, input or output | $\begin{aligned} & \mathrm{VO}_{\mathrm{EN}}=4 \mathrm{~V}, \mathrm{f}=200 \mathrm{kHz} \\ & \mathrm{CL=}=7 \mathrm{pF}, \mathrm{RL}=1 \mathrm{k} \\ & \mathrm{VS}=3 \mathrm{Vrms}, \mathrm{TA}=25 \mathrm{C} \end{aligned}$ | -45 |  | -59 | dB |
| $t_{D}$ | break before make time delay | $\mathrm{CL}=50 \mathrm{pF}$, RL=1k | 25 |  | 50 | ns |
| $\mathrm{t}_{\text {O }}$ | prop delay, address inputs to I/O channels | $\mathrm{CL}=50 \mathrm{pF}$, RL=10M |  | 0.6 | 0.4 | $\mu \mathrm{S}$ |
| $t_{\text {OfF }}$ | prop delay, address inputs to I/O channels | $\mathrm{CL}=50 \mathrm{pF}$, RL=10M |  | 0.6 | 0.4 | $\mu \mathrm{s}$ |
| $t_{\text {ONEN }}$ | prop delay, enable to I/O channels | $\mathrm{CL}=50 \mathrm{pF}$, RL=1k |  | 0.4 | 0.2 | $\mu \mathrm{S}$ |
| $\dagger_{\text {OfFFEN }}$ | prop delay, enable to I/O channels | $\mathrm{CL}=50 \mathrm{pF}$, RL=1k |  | 0.6 | 0.4 | $\mu \mathrm{S}$ |

## Truth Table

| A3 | A2 | A1 | AO | ENABLE | ON CHANNEL |
| :---: | :---: | :---: | :---: | :---: | :---: |
| X | X | X | X | H | NONE |
| L | L | L | L | L | 1 |
| L | L | L | H | L | 2 |
| L | L | H | L | L | 3 |
| L | L | H | H | L | 4 |
| L | H | L | L | L | 5 |
| L | H | L | H | L | 6 |
| L | H | H | L | L | 7 |
| L | H | H | H | L | 8 |
| H | L | L | L | L | 9 |
| H | L | L | H | L | 10 |
| H | L | H | L | L | 11 |
| H | L | H | H | L | 12 |
| H | H | L | L | L | 13 |
| H | H | L | H | L | 14 |
| H | H | H | L | L | 15 |
| H | H | H | H | L | 16 |

## Dynamic Burn-In Circuit



NOTES:
$+\mathrm{VS}=+5.5 \mathrm{~V} \pm 0.25 \mathrm{~V},-\mathrm{VS}=-5.5 \mathrm{~V} \pm 0.25 \mathrm{~V}$
$\mathrm{R}=1 \mathrm{k} \Omega \pm 5 \%$
$\mathrm{Cl}=\mathrm{C} 2=0.01 \mu \mathrm{~F} \pm 10 \%$, 1 each per socket min
D1 = D2 = IN4002, 1 each per board minimum
Input Signals: square wave, $50 \%$ duty cycle, OV to 5 V peak $\pm 10 \%$
$\mathrm{Fl}=100 \mathrm{kHz} ; \mathrm{F} 2=\mathrm{Fl} / 2 ; \mathrm{F} 3=\mathrm{Fl} / 4 ; \mathrm{F} 4=\mathrm{Fl} / 8$; $\mathrm{F} 5=\mathrm{F} 1 / 16$

## Static Burn-In Circuit



Die Pad Locations


## Structural Information

| Die Dimensions.................. $86 \times 200 \times 20$ |  |
| :---: | :---: |
| Metallization |  |
| Type.. | ..TiW/AI/Ti |
| Thickness. | .... 9.8 k ¢ $\pm 1 \mathrm{k} \AA$ |
| Glassivation |  |
| Type... | .. $\mathrm{SIO}_{2}$ |
| Thickness. | .... 8 k Å $\pm 1 \mathrm{k} \AA$ |
| Process.... | .....PCB 40 RH |

## Ordering Information

To order the Northrop Grumman radiation hardened 16:1 Analog Multiplexer, use the following part numbers. NGCL3571

(C) Commercial Flow
(B) MIL -STD -883A Class B Flow
(H) Modified Hi Rel Flow
(K) Class K Flow
(F) 28 pin flatpack
(D) Bare Die

## Approved

Unlimited Public Release


# RADIATION hardentd 16:1 ANALOG MULTIPLEXER 

NGCL3590

## Introduction

The NGCL3590 is the subject of this data sheet. However, other members of this device family are discussed in this paragraph for reference. Data sheets are available for the NGCL3571, NGCL3590, and NGCP3580. NGC3571/3580/3590 series is a family of radiation hardened 16:1 Analog Multiplexers designed by the Northrop Grumman Advanced Technology Center, Baltimore MD, using $5 \mathrm{~V}, 10 \mathrm{~V}$ and 30 V CMOS technologies on Silicon On Insulator (SOI) starting material. The NGCL3571 / NGCL3590 use a low voltage ( $10 \mathrm{~V} / 5 \mathrm{~V}$ ) process and feature CMOS analog switches. The NGCP3580 uses a high voltage (30V) process and features PMOS analog switches. CMOS analog switches result in rail to rail operation with minimal variation in switch impedance. CMOS switches offer the advantage of low switch impedance (<500 Ohms) and fast access time (<500 ns) over temperature, voltage and radiation level. All switches maintain high OFF state impedance even under power down conditions for redundant applications. SOI technology coupled with special design techniques makes this part immune to latch-up. Part has no latched data and is not subject to Single Event Upset (SEU) failures.

## Features

- 5 V CMOS using SOI starting material
- Recommended Operating Voltages $\mathrm{V}+=+5 \mathrm{~V}$, Vdig $=+5 \mathrm{~V}, \mathrm{~V}-=0 \mathrm{~V}(+/-10 \%)$
- Total Dose up to 300 krad (Si)
- No Single Event Upset (SEU) effects (no latched data)
- CMOS analog switching allows rail to rail operation and low switch impedance.
- < 700 Ohm nominal CMOS switch impedance
- < 1000 Ohm worst case CMOS switch impedance
- Break before make switching
- < 500 ns access time over temperature and post rad
- > 100 MOhm OFF switch impedance
- High OFF state impedance maintained under powered down conditions - ideal for redundant applications
- Low power dissipation: <100 $\mu \mathrm{A}$ standby current
- > 1kV electrostatic discharge protection (Human Body Model)
- Available in 28 pin flatpacks or bare die
- Full military operating temperature range, screened to specific test methods for commercial, Class B, or modified Hi Rel.


## Absolute Maximum Ratings

|  | NGCL3590 | UNITS |
| :--- | :---: | :---: |
| Supply Voltage, V+ to V- | 7.5 | volts |
| Supply Voltage, V+ to GND | 7.5 | volts |
| Supply Voltage, VDIG to GND | 7.5 | volts |
| Digital input overvoltage range min | -0.5 |  |
| Digital input overvoltage range max | V $_{\text {DIG }}+0.5$ | volts |
| Analog input overvoltage range min | V- minus 0.5 | volts |
| Analog input overvoltage range max | V+ plus 2.5 | volts |
| Storage Temperature |  |  |
| Min | -65 | deg C |
| Max | 150 | deg C |



Functional Diagram


## DC Operating Characteristics: NGCL3590

Recommended Operating Conditions: V+=+5 V, Vdig=+5V, V - = OV (+/-10\%)

| Symbol | Description | 25C Max | $\begin{aligned} & -55 \text { to }+125 \mathrm{C} \text { Max } \\ & \text { (Note 3) } \end{aligned}$ | Units |
| :---: | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\text {SUPPIY }+}$ | V+ supply current | 500 | 500 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {Supply }}$ | V-supply current | 500 | 500 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {STBY }+}$ | V+ standby current | 500 | 500 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {STBY- }}$ | V-standby current | 500 | 500 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {AH }}$ | input leakage | 1 | 1 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {AL }}$ | input leakage | 1 | 1 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {SIOFF)- }}$ | leakage into source of off switch $-v_{\text {in }}$ | 50 | 50 | nA |
| $\mathrm{I}_{\text {S(OFF)+ }}$ | leakage into source of off switch $+v_{\text {in }}$ | 50 | 50 | nA |
| $\mathrm{I}_{\text {SIOFF, Poweroff) }}$ | leakage into source of off switch, $\mathrm{v}+=\mathrm{v}-=0$ | 50 | 50 | nA |
| $\mathrm{I}_{\text {S(OFF) }} \mathrm{OV}+$ | Isoff with overvoltage | 1000 | 1000 | nA |
| $\mathrm{I}_{\text {SIOFF }} \mathrm{OV}-$ | Isoff with overvoltage | N/A (Note 1) | N/A (Note 1) | nA |
| $\mathrm{I}_{\text {D(OFF }} \mathrm{OV}+$ | leakage into drain of off switch with overvoltage | 1 | 10 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {DIOFF }} \mathrm{OV}-$ | leakage into drain of off switch with overvoltage | N/A (Note 1) | N/A (Note 1) | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {D(OFF) }}+$ | leakage into drain of off switch | 50 | 5000 | nA |
| $\mathrm{I}_{\text {D(Off) }}$ - | leakage into drain of off switch | 50 | 5000 | nA |
| $\mathrm{I}_{\text {DION) }}+$ | leakage from on driver into switch $+\mathrm{V}_{\text {in }}$ | 50 | 5000 | nA |
| $\mathrm{I}_{\text {DION) }}$ - | leakage from on driver into switch $-v_{\text {in }}$ | 50 | 5000 | nA |
| $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})} 5$ | switch on resistance $+\mathrm{V}_{\text {in }}$ | 1000 | 1000 | ohms |
| $\mathrm{R}_{\text {DS (ON) }} 0$ | switch on resistance $-\mathrm{V}_{\text {in }}$ | 1000 | 1000 | ohms |
| $\mathrm{R}_{\text {DS (ON) }}-5$ | switch on resistance $\mathrm{v}_{\text {in }}=0$ | N/A | N/A | ohms |
| $\begin{aligned} & \mathrm{R}_{\mathrm{DS}(\mathrm{ON})} \mathrm{O} \\ & \text { Delta } \end{aligned}$ | \% Nominal $\mathrm{R}_{\text {DSION }} 0 \leq \mathrm{R}_{\text {DSSoN }} 0$ (Max Measurement) $-R_{\text {osion }} 0$ (Min Measurement) | 10 (Note 2) | N/A | \% |

Note 1: The NGCL3590 does not allow undervoltage operation and maximum recommended undervoltage condition is 0.5 V below V -.

Note 2: Parameter not evaluated and is guaranteed by design
Note 3: $\quad$ Deliverable die are not tested cold and hot. Performance over temperature is guaranteed by design. Die from each wafer are sampled and tested over temperature in packages during the Class K screening.

## AC Operating Characteristics: NGCL3590

Guaranteed by design but not tested
Recommended Operating Conditions: Vdig $=5 \mathrm{~V}+/-10 \%, \mathrm{~V}+5 \mathrm{~V}+/-10 \%, \mathrm{~V}-=\mathrm{OV}$

| Symbol | Description | Conditions | -55 to +125C Limits |  | $\begin{gathered} \text { Type } \\ 25 \mathrm{C} \end{gathered}$ | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Max |  |  |
| $\mathrm{C}_{\mathrm{A}}$ | capacitance, digital Input | $\begin{aligned} & V+=V-=O V \\ & f=1 M H z, T A=25 C \end{aligned}$ |  | 7 | 1 | pF |
| $\mathrm{C}_{\text {SIoff) }}$ | capacitance, channel Input | $\begin{aligned} & V+=V-=O V \\ & f=1 M H z, T A=25 C \end{aligned}$ |  | 5 | 3 | pF |
| $\mathrm{C}_{\text {D(OFF) }}$ | capacitance, channel output | $\begin{aligned} & \mathrm{V}+=\mathrm{V}-=\mathrm{O} \\ & \mathrm{f}=\mathrm{MHz}, \mathrm{TA}=25 \mathrm{C} \end{aligned}$ |  | 50 | 30 | pF |
| $\mathrm{V}_{\text {ISO }}$ | Off isolation, input or output | $\begin{aligned} & \mathrm{VO}_{\text {EN }}=4 \mathrm{~V}, \mathrm{f}=200 \mathrm{kHz} \\ & \mathrm{CL}=7 \mathrm{pF}, \mathrm{RL}=1 \mathrm{k} \\ & \mathrm{VS}=3 \mathrm{Vrms}, \mathrm{TA}=25 \mathrm{C} \end{aligned}$ | -45 |  | -60 | dB |
| $t_{\text {D }}$ | break before make time delay | $\mathrm{CL}=50 \mathrm{pF}$, RL=1k | 25 |  | 50 | ns |
| $t_{\text {ON }}$ | prop delay, address inputs to I/O channels | CL=50pF, RL=10M |  | 0.6 | 0.4 | $\mu \mathrm{s}$ |
| $t_{\text {OfF }}$ | prop delay, address inputs to I/O channels | $\mathrm{CL}=50 \mathrm{pF}$, RL=10M |  | 0.6 | 0.4 | $\mu \mathrm{s}$ |
| $\dagger_{\text {ONEN }}$ | prop delay, enable to I/O channels | CL=50pF, RL=lk |  | 0.4 | 0.2 | $\mu \mathrm{s}$ |
| $\dagger_{\text {Offen }}$ | prop delay, enable to I/O channels | $\mathrm{CL}=50 \mathrm{pF}$, RL=1k |  | 0.6 | 0.4 | $\mu \mathrm{s}$ |

## Truth Table

| A3 | A2 | A1 | A0 | ENABLE | ON CHANNEL |
| :---: | :---: | :---: | :---: | :---: | :---: |
| X | X | X | X | H | NONE |
| L | L | L | L | L | 1 |
| L | L | L | H | L | 2 |
| L | L | H | L | L | 3 |
| L | L | H | H | L | 4 |
| L | H | L | L | L | 5 |
| L | H | L | H | L | 6 |
| L | H | H | L | L | 7 |
| L | H | H | H | L | 8 |
| H | L | L | L | L | 9 |
| H | L | L | H | L | 10 |
| H | L | H | L | L | 11 |
| H | L | H | H | L | 12 |
| H | H | L | L | L | 13 |
| H | H | L | H | L | 14 |
| H | H | H | L | L | 15 |
| H | H | H | H | L | 16 |

## Dynamic Burn-In Circuit



## Static Burn-In Circuit



Die Pad Locations


Structural Information
Die Dimensions $\qquad$ $86 \times 200 \times 20$ mils

Die Attach
$\qquad$ Gold Eutectic
Metallization
Type. $\qquad$
Thickness $\qquad$ $9.8 \mathrm{kÅ} \pm 1 \mathrm{kÅ}$ Material
Temperature $\qquad$ $400^{\circ} \mathrm{C}$
Lead Temperature $<275^{\circ} \mathrm{C}$ (10 sec soldering)

Glassivation
Type $\mathrm{SiO}_{2}$
Thickness 8 k Â $\pm 1 \mathrm{k} \AA$
Process $\qquad$ PCB 40 RH (with 5V gate oxide process module)

## Ordering Information

To order the Northrop Grumman radiation hardened 16:1 Analog Multiplexer, use the following part numbers.
NGCL3590

(-) No total dose screening
(M) 50 kRad (Si)
(P) 150 kRad (Si)
(T) 300 kRad (Si)
(C) Commercial Flow
(B) MIL -STD -883A Class B Flow
(H) Modified Hi Rel Flow
(K) Class K Flow
(F) 28 pin flatpack
(D) Bare Die

## Approved

Unlimited Public Release


## Introduction

The NGCP3580 is the subject of this data sheet. However, other members of this device family are discussed in this paragraph for reference. Data sheets are available for the NGCL3571, NGCL3590, and NGCP3580. NGC3571/3580/3590 series is a family of radiation hardened 16:1 Analog Multiplexers designed by the Northrop Grumman Advanced Technology Center, Baltimore, MD, using $5 \mathrm{~V}, 10 \mathrm{~V}$ and 30 V CMOS technologies on Silicon On Insulator (SOI) starting material. The NGCL3571 and NGCL3590 use a low voltage ( $10 \mathrm{~V} / 5 \mathrm{~V}$ ) process and feature CMOS analog switches. The NGCP3580 uses a high voltage (30V) process and features PMOS analog switches. All switches maintain high OFF state impedance even under power down conditions for redundant applications. SOI technology coupled with special design techniques makes this part immune to latch-up. Part has no latched data and is not subject to Single Event Upset (SEU) failures.

## Features

- CMOS using SOI starting material
- Recommended Operating Voltages $\mathrm{V}+=15 \mathrm{~V}$, Vdig $=+5 \mathrm{~V}, \mathrm{~V}-=-15 \mathrm{~V}$ (+/-10\%)
- Total Dose up to 300 krad (Si)
- No Single Event Upset (SEU) effects (no latched data)
- < 800 Ohm nominal PMOS switch impedance
- < 1500 Ohm worst case PMOS switch impedance
- Break before make switching
- < 500 ns access time over temperature and post rad
- > 100 MOhm OFF switch impedance
- High OFF state impedance maintained under powered down conditions - ideal for redundant applications
- Low power dissipation: <100 $\mu \mathrm{A}$ standby current
- > lkV electrostatic discharge protection (Human Body Model)
- Available in 28 pin flatpacks or bare die
- Full military operating temperature range, screened to specific test methods for commercial, Class B, or modified Hi Rel.


## Absolute Maximum Ratings

|  | NGCP3580 | UNITS |
| :--- | :---: | :---: |
| Supply Voltage, V+ to V- | 40 | volts |
| Supply Voltage, V+ to GND | 20 | volts |
| Supply Voltage, VDIG to GND | 7.5 | volts |
| Digital input overvoltage range min | -0.5 |  |
| Digital input overvoltage range max | V $_{\text {DIG }}+0.5$ | volts |
| Analog input overvoltage range min | V- minus 10 | volts |
| Analog input overvoltage range max | V+ plus 10 | volts |
| Storage Temperature |  |  |
| Min | -65 | deg C |
| Max | 150 | deg C |



## Functional Diagram



## DC Operating Characteristics: NGCP3580

Recommended Operating Conditions: V $+=+15+/-10 \% \mathrm{~V}, \mathrm{~V}-=-15+/-10 \% \mathrm{~V}, \mathrm{Vdig}=+5+/-10 \% \mathrm{~V}$

| Symbol | Description | 25C Max | $\begin{aligned} & -55 \text { to }+125 \mathrm{C} \text { Max } \\ & \text { (Note 1) } \end{aligned}$ | Units |
| :---: | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\text {SUPPIY }+}$ | V+ supply current | 500 | 500 | $\mu \mathrm{A}$ |
| $I_{\text {supply }}$ | V-supply current | 500 | 500 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {SBYY }+}$ | V+ standby current | 500 | 500 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {STBY- }}$ | V-standby current | 500 | 500 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {AH }}$ | input leakage | 1 | 1 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\mathrm{AL}}$ | input leakage | 1 | 1 | UA |
| $-_{\text {SIOFFI- }}$ | leakage into source of off switch $-v_{\text {in }}$ | 50 | 500 | nA |
| $+\mathrm{I}_{\text {S(OFF) }}$ | leakage into source of off switch $+v_{\text {in }}$ | 50 | 500 | nA |
| $\mathrm{I}_{\text {SIOFF, POWEROFFI }}$ | leakage into source of off switch, $\mathrm{v}+=\mathrm{v}-=0$ | 50 | 2000 | nA |
| $\mathrm{I}_{\text {SIOFF }} \mathrm{OV}+$ | Isoff with overvoltage | 1 | 20 | UA |
| $\mathrm{I}_{\text {S(OFF) }} \mathrm{OV}-$ | Isoff with overvoltage | 1 | 1 | UA |
| $\mathrm{I}_{\text {D(OFF }} \mathrm{OV}+$ | leakage into drain of off switch with overvoltage | 1 | 30 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {D(OFF) }} \mathrm{OV}-$ | leakage into drain of off switch with overvoltage | 1 | 10 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {D(OFF) }}+$ | leakage into drain of off switch | 50 | 5000 | nA |
| $\mathrm{I}_{\text {D(Off) }}$ - | leakage into drain of off switch | 50 | 5000 | nA |
| $\mathrm{I}_{\text {DION) }}+$ | leakage from on driver into switch $+\mathrm{v}_{\text {in }}$ | 50 | 5000 | nA |
| $\mathrm{I}_{\text {DION) }}$ - | leakage from on driver into switch $-\mathrm{v}_{\text {in }}$ | 50 | 5000 | nA |
| $\mathrm{R}_{\text {DSION }} 15$ | switch on resistance $+\mathrm{V}_{\text {in }}$ | 800 | 800 | ohms |
| $\mathrm{R}_{\mathrm{DS} \text { (ON) }} 5$ | switch on resistance $v_{\text {in }}=5$ | 1500 | 1500 | ohms |
| $\mathrm{R}_{\mathrm{DS} \text { (ON) }} 0$ | switch on resistance $v_{\text {in }}=0$ | 1500 | 1500 | ohms |

Note 1: Deliverable die are not tested cold and hot. Performances over temperature are guaranteed by design. Die from each wafer are sampled over temperature in packages during the Class K screening.

## AC Operating Characteristics: NGCP3580

Guaranteed by design but not tested
Recommended Operating Conditions: $\mathrm{V}+=+15 \mathrm{~V}+/-10 \%, \mathrm{~V}-=-15 \mathrm{~V}+/-10 \%, \mathrm{~V}_{\text {dig }}=+5 \mathrm{~V}+/-10 \%$

| Symbol | Description | Condifions | -55 to +125C Limits |  | туре 25C | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Max |  |  |
| $\mathrm{C}_{\text {A }}$ | capacitance, digital input | $\begin{aligned} & V+=V-=O V \\ & f=1 M H z, T A=25 C \end{aligned}$ |  | 7 | 1 | pF |
| $\mathrm{C}_{\text {S(Iff) }}$ | capacitance, channel input | $\begin{aligned} & V+=V-=O V \\ & f=1 \mathrm{MHz}, \mathrm{TA}=25 \mathrm{C} \end{aligned}$ |  | 5 | 3 | pF |
| $\mathrm{C}_{\text {D(OFF) }}$ | capacitance, channel output | $\begin{aligned} & \mathrm{V}+=\mathrm{V}-=\mathrm{O} \\ & \mathrm{f}=1 \mathrm{MHz}, \mathrm{TA}=25 \mathrm{C} \end{aligned}$ |  | 50 | 30 | pF |
| $V_{\text {ISO }}$ | off isolation, input or output | $\begin{aligned} & \mathrm{VO}_{\text {EN }}=4 \mathrm{~V}, \mathrm{f}=200 \mathrm{kHz} \\ & \mathrm{CL=} 7 \mathrm{pF}, \mathrm{RL}=1 \mathrm{k} \\ & \mathrm{VS}=3 \mathrm{Vrms}, \mathrm{TA}=25 \mathrm{C} \end{aligned}$ | -45 |  | -59 | dB |
| $t_{0}$ | break before make time delay | $\mathrm{CL}=50 \mathrm{pF}$, RL=1k | 25 |  | 50 | ns |
| $t_{\text {ON }}$ | prop delay, address inputs to I/O channels | $\mathrm{CL}=50 \mathrm{pF}$, RL=10M |  | 0.6 | 0.4 | $\mu \mathrm{s}$ |
| $t_{\text {OfF }}$ | prop delay, address inputs to I/O channels | $\mathrm{CL}=50 \mathrm{pF}$, RL=10M |  | 0.6 | 0.4 | $\mu \mathrm{s}$ |
| $\dagger_{\text {ONEN }}$ | prop delay, enable to I/O channels | $\mathrm{CL}=50 \mathrm{pF}$, RL=1k |  | 0.4 | 0.2 | $\mu \mathrm{s}$ |
| $\dagger_{\text {Offen }}$ | prop delay, enable to I/O channels | $\mathrm{CL}=50 \mathrm{pF}$, RL=1k |  | 0.6 | 0.4 | $\mu \mathrm{s}$ |

## Truth Table

| A3 | A2 | A1 | AO | ENABLE | ON CHANNEL |
| :---: | :---: | :---: | :---: | :---: | :---: |
| X | X | X | X | H | NONE |
| L | L | L | L | L | 1 |
| L | L | L | H | L | 2 |
| L | L | H | L | L | 3 |
| L | L | H | H | L | 4 |
| L | H | L | L | L | 5 |
| L | H | L | H | L | 6 |
| L | H | H | L | L | 7 |
| L | H | H | H | L | 8 |
| H | L | L | L | L | 9 |
| H | L | L | H | L | 10 |
| H | L | H | L | L | 11 |
| H | L | H | H | L | 12 |
| H | H | L | L | L | 13 |
| H | H | L | H | L | 14 |
| H | H | H | L | L | 15 |
| H | H | H | H | L | 16 |

## Dynamic Burn-In Circuit



NOTES:
$+\mathrm{VS}=+16.5 \mathrm{~V} \pm 0.25 \mathrm{~V},-\mathrm{VS}=-16.5 \mathrm{~V} \pm .025 \mathrm{~V}$
$R=1 k \Omega \pm 5 \%$
$\mathrm{Cl}=\mathrm{C} 2=0.01 \mu \mathrm{~F} \pm 10 \%$, 1 each per socket min
D1 = D2 = IN4 002, 1 each per board minimum
Input Signals: square wave, 50\% duty cycle,
OV to 5V peak $\pm 10 \%$
$\mathrm{Fl}=100 \mathrm{kHz} ; \mathrm{F} 2=\mathrm{Fl} / 2 ; \mathrm{F} 3=\mathrm{Fl} / 4 ; \mathrm{F} 4=\mathrm{Fl} / 8 ; \mathrm{F} 5=\mathrm{Fl} / 16$

## Static Burn-In Circuit




Structural Information

| Die Dimensions.................. $86 \times 200 \times 20$ |  |
| :---: | :---: |
| Metallization |  |
| тype........ | .TiW/Al/Ti |
| Thickness.. | .9.8 K A $\pm 1 \mathrm{k}$ 过 |
| Glassivation |  |
| Type...... | . $\mathrm{SiO}_{2}$ |
| Thickness.. | . 8 k Å $\pm 1 \mathrm{kA}$ |
| Process..... | .PCB 40 RH |

Die Attach
Material $\qquad$ Gold Eutectic
Temperature $\qquad$ $400^{\circ} \mathrm{C}$
Lead Temperature $<275^{\circ} \mathrm{C}$ (10 sec soldering)

## Ordering Information

To order the Northrop Grumman radiation hardened 16:1 Analog Multiplexer, use the following part numbers. NGCP3580

(-) No total dose screening
(M) 50 kRad (Si)
(P) 150 kRad (Si)
(T) 300 kRad (Si)
(C) Commercial Flow
(B) MIL -STD -883A Class B Flow
(H) Modified Hi Rel Flow
(K) Class K Flow
(F) 28 pin flatpack
(D) Bare Die

## Approved

Unlimited Public Release

