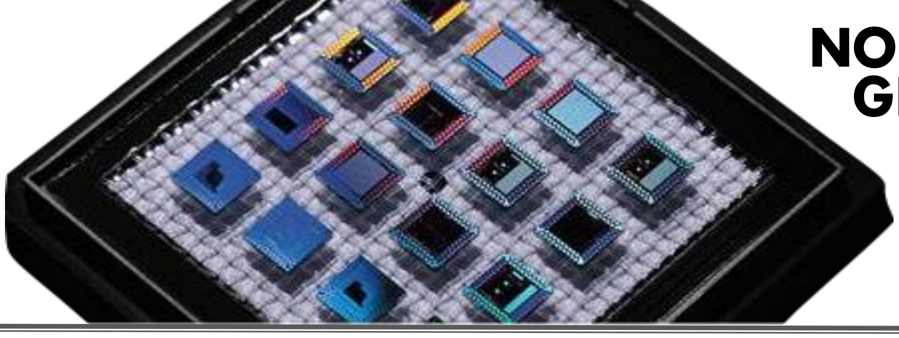
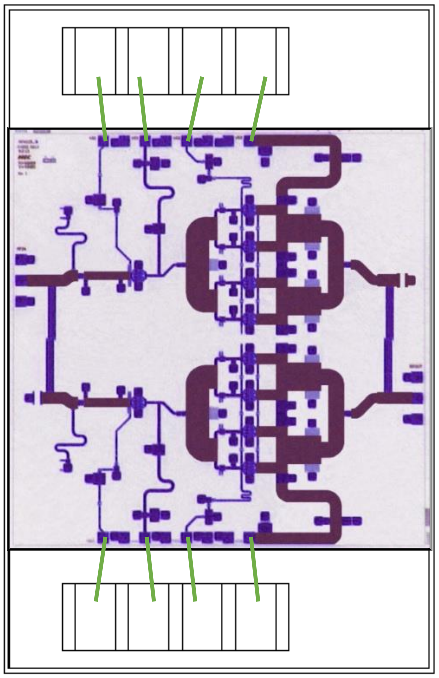
APN228TAB
27 – 31 GHz
GaN Power Amp
On Tab

Revision 2023-1





Size = 6.35mm x 4.09mm (0.250" x 0.161")

Product Description

The APN228TAB monolithic GaN HEMT amplifier die on tab is a broadband, two-stage power device, designed for use in SATCOM Terminals and point-to-point digital radios. The APN228TAB is a APN228 die that has been attached with eutectic solder to a copper molybdenum based (CuMoCu-based) tab and is pre-assembled with 100pF, 100V shunt capacitors for the circuit's bias. The Gold plated bond pads are compatible with both manual and automatic gold wire bonders. The CuMoCu based tab is compatible with epoxy and eutectic die attach methods.

Applications

- Point-to-Point Digital Radios
- Point-to-Multipoint Digital Radios
- SatCom Terminals

Product Features

- RF frequency: 27 to 31 GHz
- Linear Gain: 16 dB typ.
- Psat: ~16 W on wafer, typical
- Psat: ~12.5 W (CW)
- Die Size: 16 sq. mm.
- 0.2um GaN HEMT Process
- 4 mil SiC substrate on 0.010" CuMoCu based tab
- DC Power: 28 VDC @ 1.2 A
- ESD Rating = Class 0 (sensitive to < 100V)

Export Information
ECCN: **3A001.b.2.c**
HTS (Schedule B) code: **8542.33.0001**

* Pulsed-Power On-Wafer unless otherwise noted

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Absolute Maximum Ratings

Parameter	Value	Unit
Drain Voltage	28	V
Gate Voltage Range	-8 to 0	V
Drain Current	1500	mA
Gate Current	0.6	mA
Power Dissipation*	42	W
Soldering Temperature	320	ºC

*7W/mm of gate periphery

Recommended Operating Conditions

Parameter	Value	Unit
Drain Voltage Range	20 - 28	V
Gate Voltage Range	-5 to -3	V
Stg 1 Drain Current (Idq)	240	mA
Stg 2 Drain Current (Idq)	240 – 960	mA

Electrical Specifications

Parameter	Min	Typ	Max	Unit
Operational Frequency	27		31	GHz
Small Signal at 28V				
Small Signal Linear Gain	18.5		20	dB
Input Return Loss	-35		-20	dB
Output Return Loss	-26		-16	dB
On-Wafer Pulsed Power at 28V				
Psat (at 27 dBm)		42		dBm
Power Gain (at 27 dBm)	19.1	19.6	20.1	dB
P1db	41.20	42	42.5	dBm
PAE (at 27 dBm)	30.5	32.5	34	%
Max PAE	31	32.9	33.8	%
Fixtured CW at 24V, 25ºC Case Temp				
Psat (at 28 dBm)	38.1	39	39.6	dBm
Power Gain (at 28 dBm)	15.3	16.9	17.8	dB
PAE (at 28 dBm)	19.1	22	24.7	%
Max PAE	24		28.4	%
Drain Voltage		28		V
Stage 1 Gate Voltage		-3.925		V
Stage 2 Gate Voltage		-3.925		V
Stage 1 Idq		240		mA
Stage 2 Idq		960		mA

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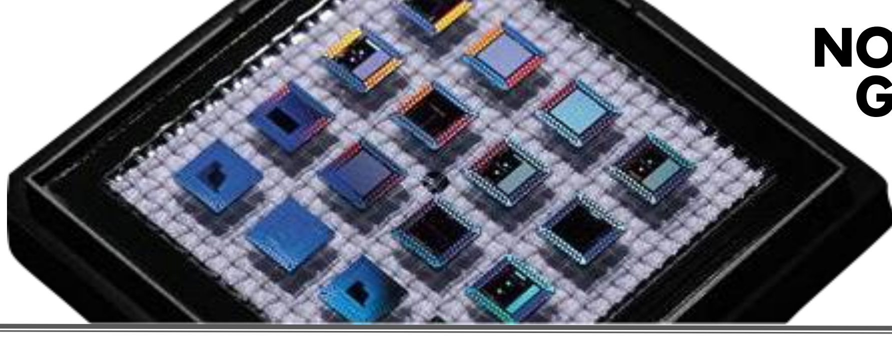

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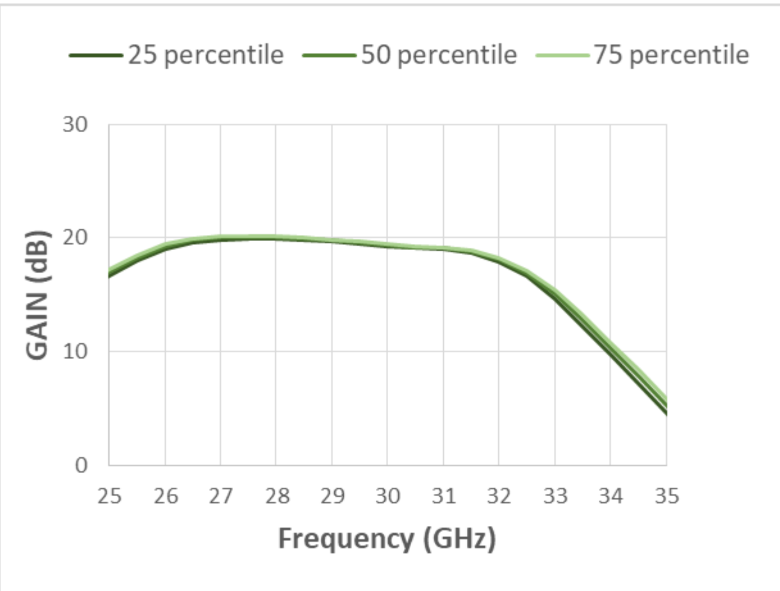
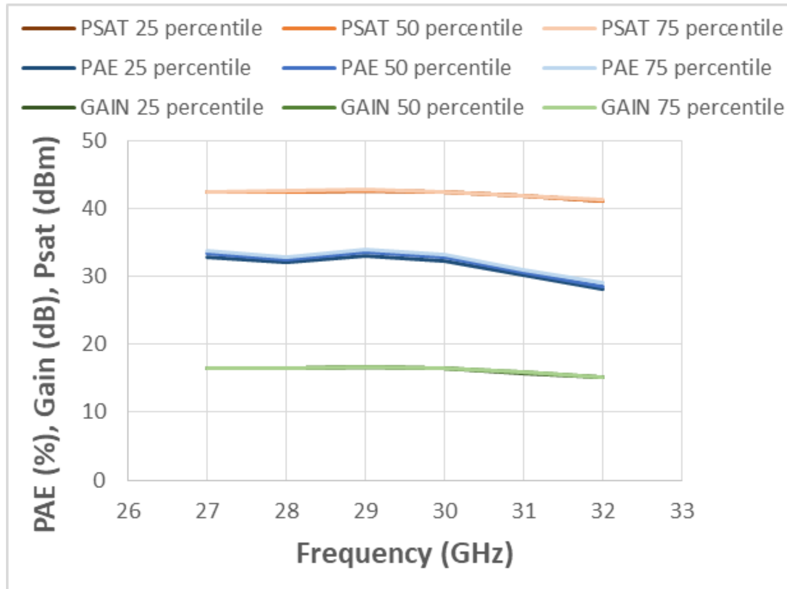
On wafer measured Performance Characteristics (Typical Performance at 25°C)
Vd = 28.0 V, Id1 + Id1a = 240mA, Id2 + Id2a =960 mA

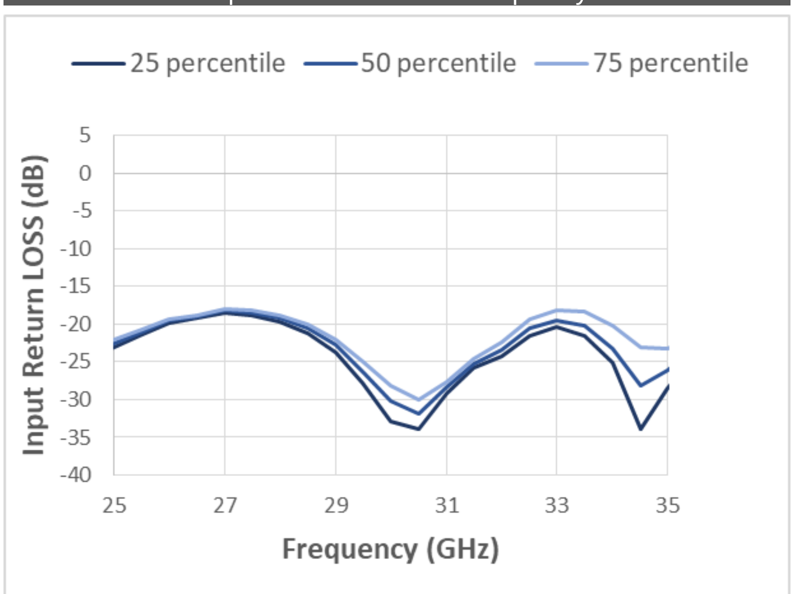
Small Signal GAIN vs. Frequency



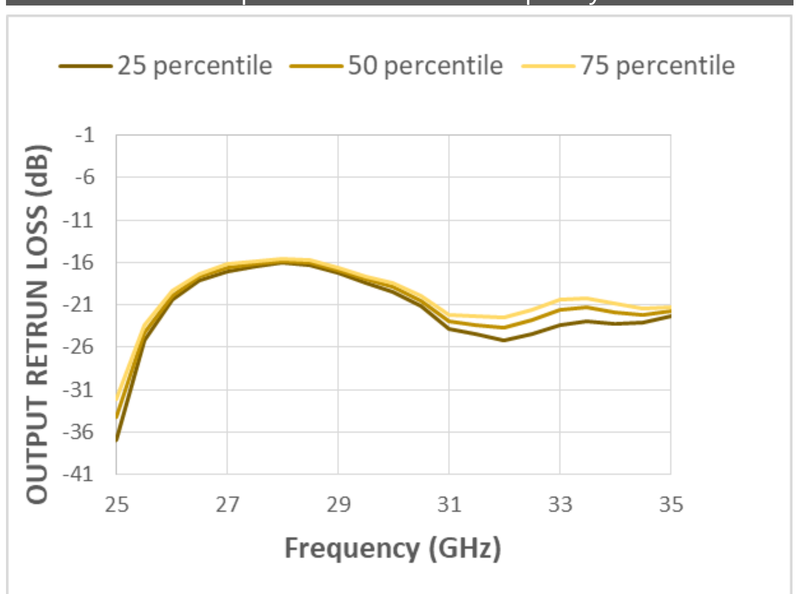
Large Signal PAE, GAIN, PSAT vs. Frequency



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



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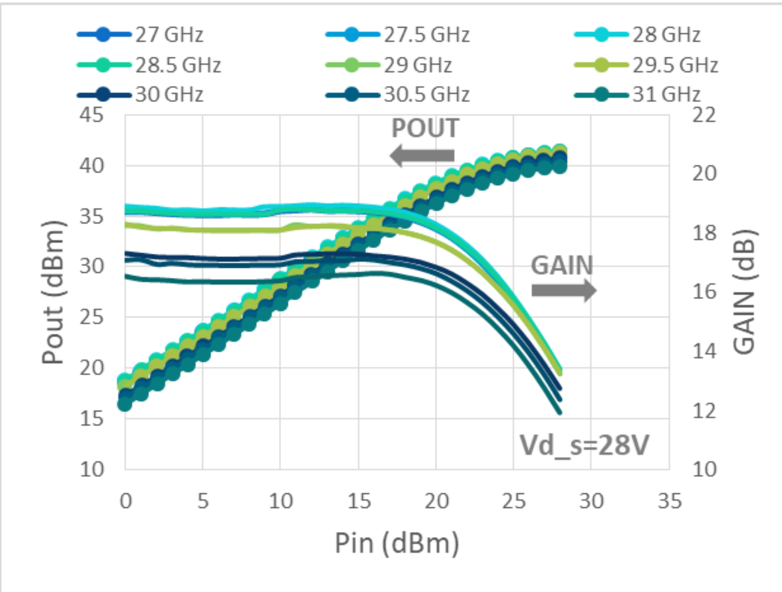
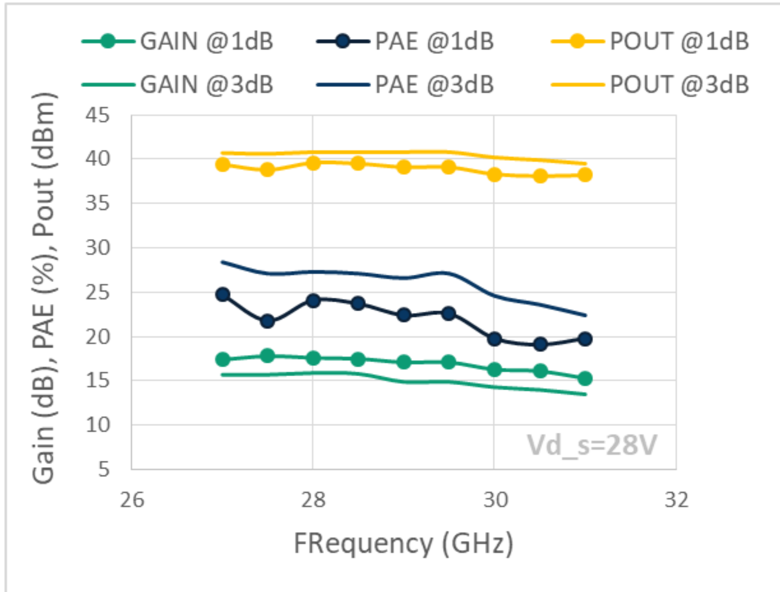
Fixture measured Performance Characteristics (Typical Performance at 25°C)
Vd = 28.0 V, Id1 + Id1a = 240mA, Id2 + Id2a =960 mA

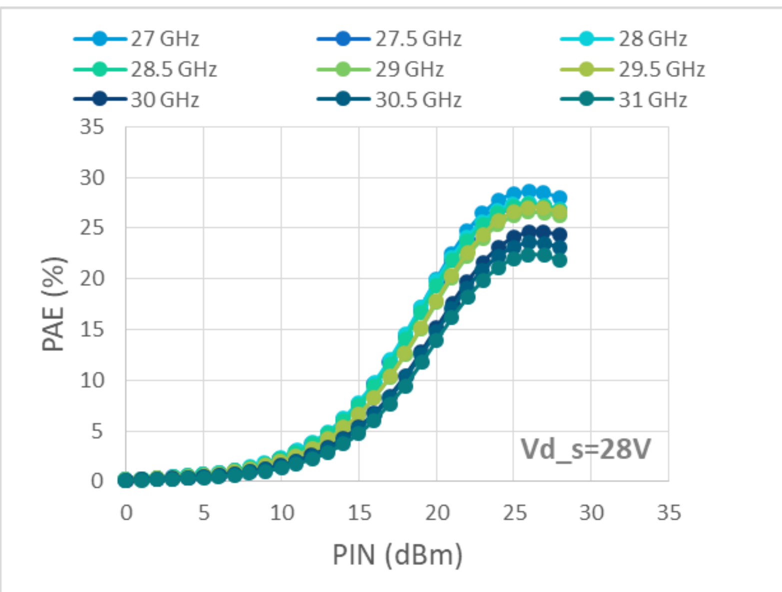
POUT and GAIN vs. PIN



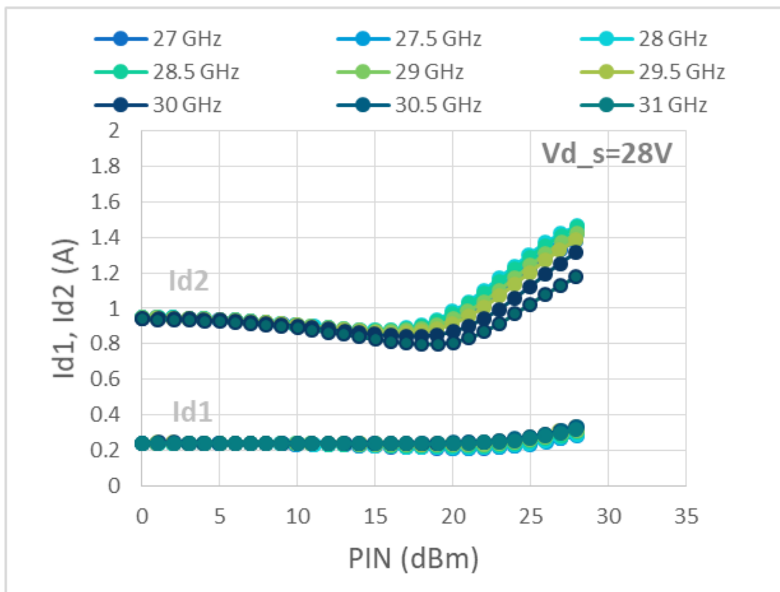
PAE, GAIN, POUT vs. FREQUENCY



PAE vs PIN



Id1, Id2 vs PIN



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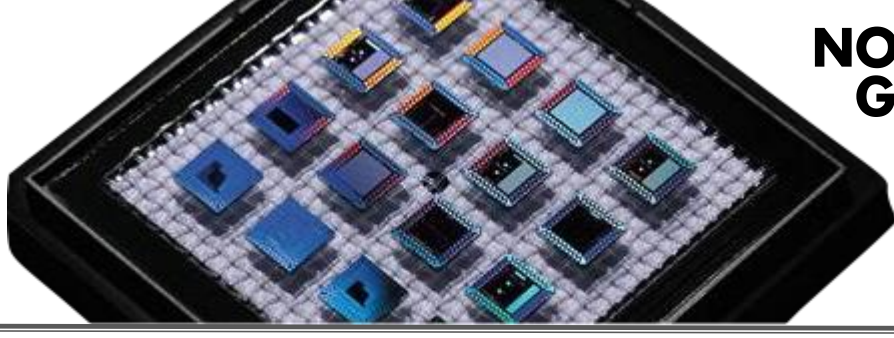

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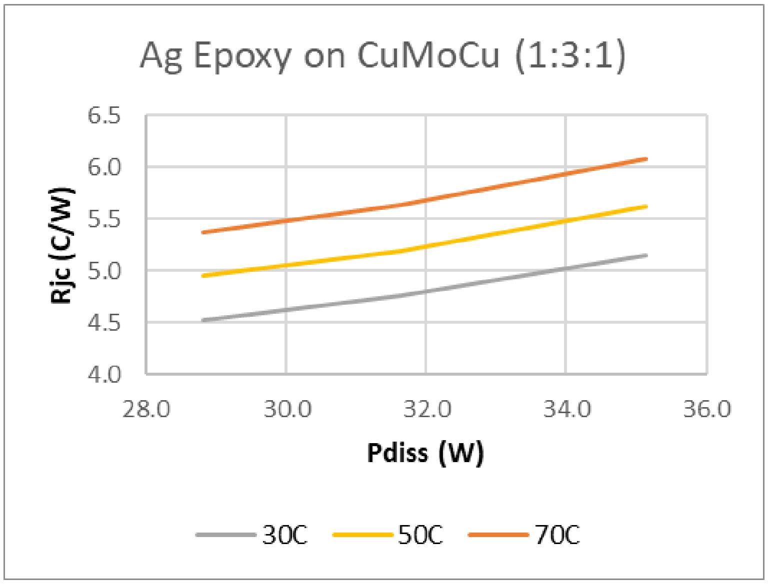
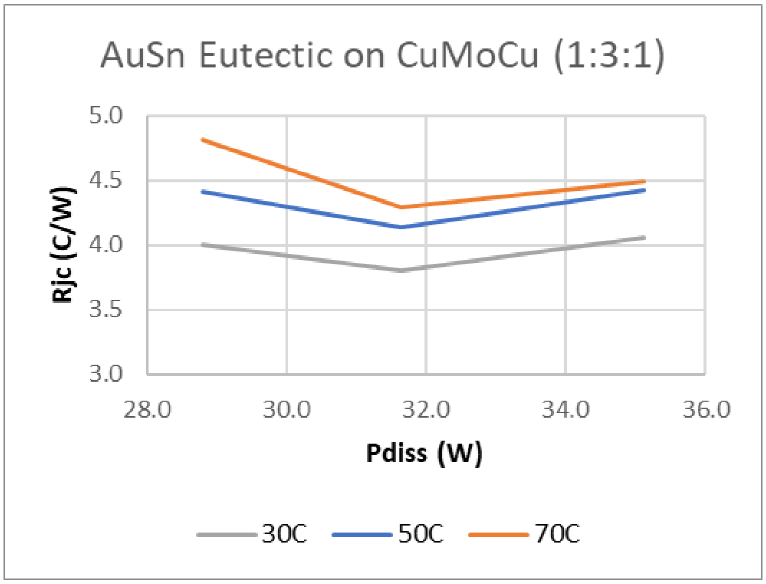
Preliminary thermal properties with die mounted with 1mil 80/20 AuSn Eutectic and 1mil Ag epoxy to 10mil CuMoCu shim

Shim	Mounting Material	Average Backside Die Temperature	Hottest Junction Temperature Tjc	RF Output (dBm)	Power Dissipation (W)	Thermal Resistance Rjc (ºC/W)
10 mil CuMoCu	AuSn Eutectic	30 ºC	145	39.8	28.8	4.0
			150	41.0	31.6	3.8
			173	41.3	35.1	4.1
		50 ºC	177	39.8	28.8	4.4
			181	41.0	31.6	4.1
			206	41.3	35.1	4.4
		70 ºC	209	39.8	28.8	4.8
			206	41.0	31.6	4.3
			228	41.3	35.1	4.5
10 mil CuMoCu	Ag Epoxy	30 ºC	160	39.8	28.8	4.5
			180	41.0	31.6	4.8
			211	41.3	35.1	5.2
		50 ºC	193	39.8	28.8	5.0
			214	41.0	31.6	5.2
			247	41.3	35.1	5.6
		70 ºC	225	39.8	28.8	5.4
			248	41.0	31.6	5.6
			284	41.3	35.1	6.1





** Vd = 28.0 V, Idq1 = 240 mA, Id2q = 960 mA

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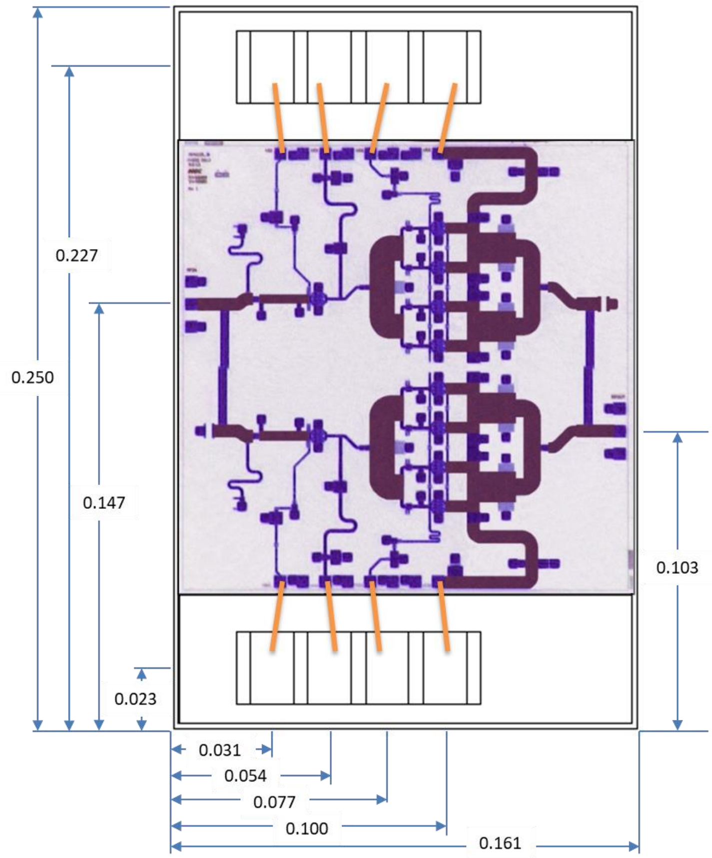
Die Size and Bond Pad Locations (Not to Scale)



<u>APN228 Die</u>
X = 4000 µm ± 25 µm (0.158” ± 0.001”)
Y = 4000 ± 25 µm (0.158” ± 0.001”)
DC Bond Pad = 100 x 100 ± 0.5 µm (0.004” nominal)
RF Bond Pad = 100 x 100 ± 0.5 µm (0.004” nominal)
Chip Thickness = 101 ± 5 µm (0.004”)

<u>CuMoCu-based Tab</u>
X = 0.161” ± 0.001” (4089 µm ± 25 µm)
Y = 0.250” ± 0.001” (6350 µm ± 25 µm)
Tab Thickness = 0.010” ± 0.001” (254 µm ± 25 µm)

<u>Eutectic Solder layer</u>
Eutectic Thickness = 1 mil (25 µm) nominal

<u>100pF, 100V Bar Capacitors</u>
X = 0.094” ± 0.003” (2388 µm ± 76 µm)
Y = 0.030” ± 0.003” (762 µm ± 76 µm)
DC Bond Pad = 0.015” x 0.026” (381 x 660 µm nominal)
Cap Thickness = 0.005” ± 0.0015” (127 µm ± 38 µm)
Cap Part Number = CRM-BN-94X30X5-G-101-Z-CE396
(or equivalent)

Biasing/De-Biasing Details:

Listed below are some guidelines for GaN device testing and wire bonding:

a. Limit positive gate bias (G-S or G-D) to < 1V
b. Know your devices’ breakdown voltages
c. Use a power supply with both voltage and current limit.
d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture.
    i. Apply negative gate voltage (-8 V) to ensure that all devices are off
    ii. Ramp up drain bias to ~10 V
    iii. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
    iv. Ramp up drain to operating bias
    v. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved
e. To safely de-bias GaN devices, start by debiasing output amplifier stages first (if applicable):
    i. Gradually decrease drain bias to 0 V.
    ii. Gradually decrease gate bias to 0 V.
    iii. Turn off supply voltages
f. Repeat de-bias procedure for each amplifier stage

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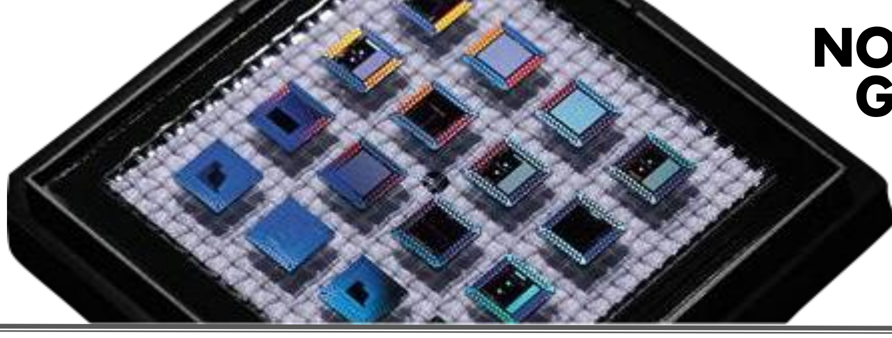
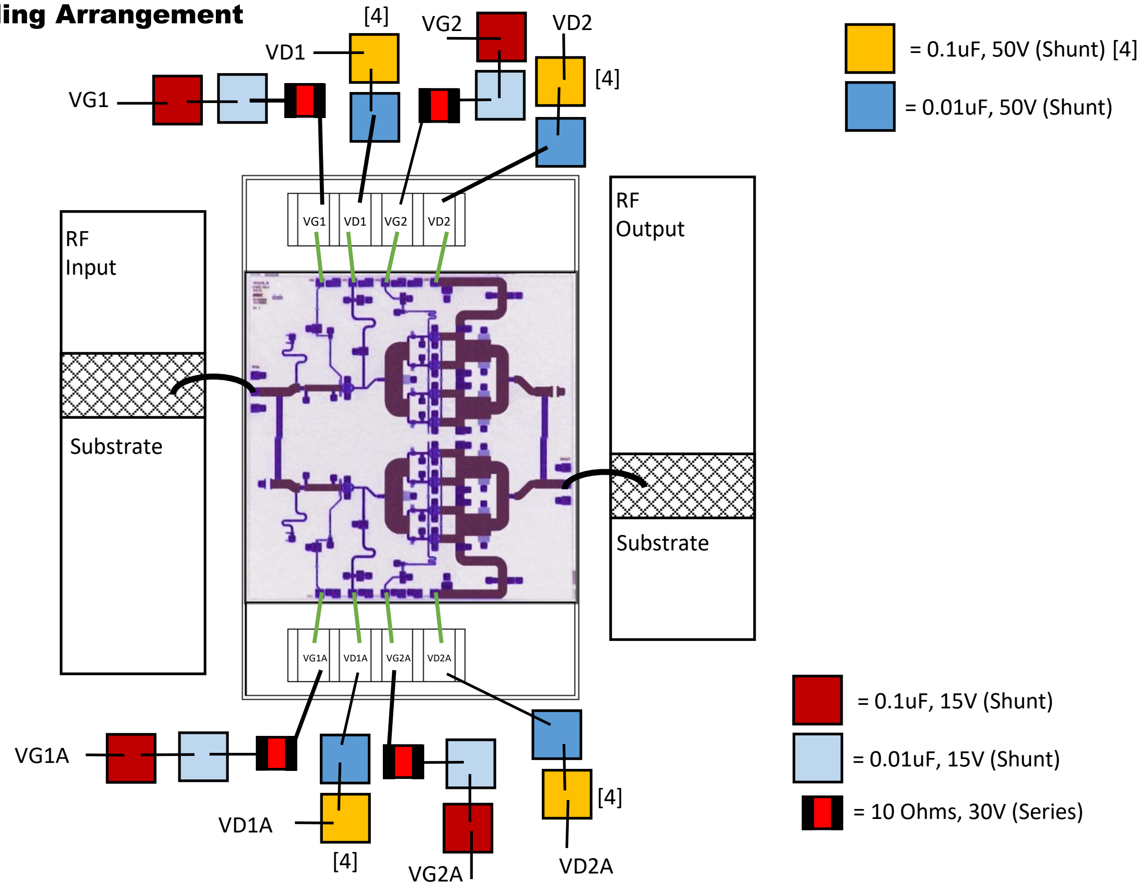


Suggested Bonding Arrangement



Recommended Assembly Notes

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
3. Part must be biased from both sides as indicated.
4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF , 50V Capacitors.

Mounting Processes

Most NGSS GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGSS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320°C for 30 seconds.

Note: Many of the NGSS parts do incorporate airbridges, so caution should be used when determining the pick up tool.

CAUTION: THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS.

PLEASE ALSO REFER TO OUR "GaN Chip Handling Application Note" BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!

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